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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,509	10/12/2001	Richard L. Hudson	42390P11897	3993

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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,509	HUDSON, RICHARD L.	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-7,9 and 11-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7,9,11 and 13-22* is/are rejected.

7)☒ Claim(s) *6 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 18-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The cited subject matter is directed toward an executable instruction set. M.P.E.P. 2106 details that a program, e.g. an instruction set, absent of the statutory computer storage medium that would embody the program is non-statutory. Therefore, the cited claims as being directed toward an instruction set without the statutory computer storage medium is non-statutory.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3, 7, 9, 13 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by HIRONO (U.S. Patent 6,910,213).

As to claim 1, HIRONO teaches a computer implemented method comprising: monitoring thread switches in a multiple-threaded application through use of a single

thread switch flag (via detecting the presence / absence of context switching); executing a non-blocking thread synchronization sequence (via exclusive executing a mutual exclusive write or read operation); interrupting the non-blocking thread synchronization sequence upon the occurrence of a thread switch (via invalidating the process of a thread); and repeating the non-blocking thread synchronization sequence, wherein the non-blocking thread synchronization sequence is idempotent in order to abandon the non-blocking thread synchronization sequence in mid-sequence without consequences (via invalidating the process of a thread in the period mentioned and re-executing the process) (col. 23, lines 59 – col. 24, line 5; abstract; col. 7, lines 29-60).

As to claim 3, HIRONO teaches the multiple-threaded applications are supported by a computer programming language selected from the group consisting of JAVA, C, LISP, and Pascal (via the program as an intermediate code such as byte code, e.g. Java, and represents various threads) (col. 20, line 49-57).

As to claims 7 and 9, reference is made to a machine readable medium that corresponds to the method of claims 1 and 3 and is therefore met by the rejection of claims 1 and 3 above.

As to claim 13, HIRONO teaches a computing system comprising: at least one central processing unit (col. 20, lines 41-42), the central processing unit executing multi-threaded applications (program) (col. 20, lines 40-57); a thread switch indicator to

indicate the occurrence of a thread switch (via detecting the presence / absence of context switching); and an instruction set to implement non-blocking thread synchronization sequences such that partially completed non-blocking thread synchronization sequences used to share resources (cpu / memory / object / garbage collector / etc.) local to the at least one central processing unit can be abandoned and repeated upon the occurrence of a thread switch (via detecting the presence / absence of context switching, invalidating the process of a thread in the period mentioned and re-executing the process) (col. 23, lines 59 – col. 24, line 5; abstract; col. 7, lines 29-60); wherein the non-blocking thread synchronization sequences are indempotent in order to abandon the non-blocking thread synchronization sequences in mid-sequence without consequences (via detecting the presence / absence of context switching, invalidating the process of a thread in the period mentioned and re-executing the process) (col. 23, lines 59 – col. 24, line 5; abstract; col. 7, lines 29-60).

As to claim 17, HIRONO teaches the computing system uses a computer programming language selected from the group consisting of JAVA, C, LISP, and Pascal (via the program as an intermediate code such as byte code, e.g. Java, and represents various threads) (col. 20, line 49-57).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 11, 14-16 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over HIRONO (U.S. Patent 6,910,213) in view of "Cycles to Recycle: Garbage Collectionon the IA-64" by HUDSON et al.

As to claim 5, HIRONO substantially discloses the invention. However, HIRONO does not teach the synchronization sequence is a frontier pointer based allocation sequence.

HUDSON teaches the performing a frontier pointer-based synchronization allocation sequence when thread switching (pg. 104, Avoiding Lock Overhead: Can the OS Help; pg. 102, "We exploit the acquire/release model in implementing Java synchronization and in achieving publication safety."). HUDSON also teaches the threads perform synchronization sequences (via the mov and st8 instructions. See page 104, 2nd column; pg. 109, section 5). Therefore, it would be obvious to one of ordinary skill in the art to combine the teachings of HIRONO with the teachings of HUDSON in order to facilitate avoidance of lock overhead (pg. 103, Object allocation; pg. 104, Avoiding Lock Overhead).

As to claim 11, reference is made to a machine readable medium that corresponds to the method of claim 5 and is therefore met by the rejection of claim 5 above.

As to claim 14, HIRONO substantially teaches the invention. However, HIRONO does not teach the cited instruction set. HUDSON teaches the instruction set includes: a set instruction to set the thread switch indicator upon the occurrence of a thread switch (4.2.2, Fig. 3), a first conditional move instruction to move data if the thread switch indicator is set (Fig. 3); a second conditional move instruction to move data if the thread switch indicator is not set (Fig. 3), a first jump instruction to bypass instructions if the thread switch indicator is set (4.2.2),a second jump instruction to bypass instructions if the thread switch indicator is not set (4.2.2); and a clear instruction to clear the thread switch indicator (Fig. 3). Therefore, it would be obvious to one of ordinary skill in the art to combine the teachings of HIRONO with the teachings of HUDSON in order to facilitate avoidance of lock overhead (pg. 103, Object allocation; pg. 104, Avoiding Lock Overhead).

As to claim 15, HIRONO teaches the thread switch indicator is a thread switch flag (abstract).

As to claim 16, HIRONO teaches at the central processing unit has a single allocation area (col. 23, lines 59 – col. 24, line 5; abstract; col. 7, lines 29-60). However, HIRONO does not teach the synchronization sequence is a frontier pointer based allocation sequence.

HUDSON teaches the performing a frontier pointer-based synchronization allocation sequence when thread switching (pg. 104, Avoiding Lock Overhead: Can the

OS Help; pg. 102, "We exploit the acquire/release model in implementing Java synchronization and in achieving publication safety."). HUDSON also teaches the threads perform synchronization sequences (via the mov and st8 instructions. See page 104, 2nd column; pg. 109, section 5). Therefore, it would be obvious to one of ordinary skill in the art to combine the teachings of HIRONO with the teachings of HUDSON in order to facilitate avoidance of lock overhead (pg. 103, Object allocation; pg. 104, Avoiding Lock Overhead).

As to claims 18 and 19, reference is made to the instruction set that corresponds to the system of claim 14 and is therefore met by the rejection of claim 14 above.

As to claim 20, HIRONO teaches the thread switch indicator is a thread switch flag (abstract).

As to claim 21, HIRONO teaches implementing a non-blocking thread synchronization sequence for executing a multithreaded application (via exclusive executing a mutual exclusive write or read operation such that if a context switch occurs invalidating the process of a thread in the period mentioned and re-executing the process) (col. 23, lines 59 – col. 24, line 5; abstract; col. 7, lines 29-60)

As to claim 22, HUDSON teaches the performing a frontier pointer-based synchronization allocation sequence when thread switching (pg. 104, Avoiding Lock

Overhead: Can the OS Help; pg. 102, "We exploit the acquire/release model in implementing Java synchronization and in achieving publication safety."). HUDSON also teaches the threads perform synchronization sequences (via the mov and st8 instructions. See page 104, 2nd column; pg. 109, section 5). Therefore, it would be obvious to one of ordinary skill in the art to combine the teachings of HIRONO with the teachings of HUDSON in order to facilitate avoidance of lock overhead (pg. 103, Object allocation; pg. 104, Avoiding Lock Overhead).

Allowable Subject Matter

6. Claims 6 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 3, 5, 7, 9, 11, and 13-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER

July 21, 2006